

After writing the first page and before writing the second page

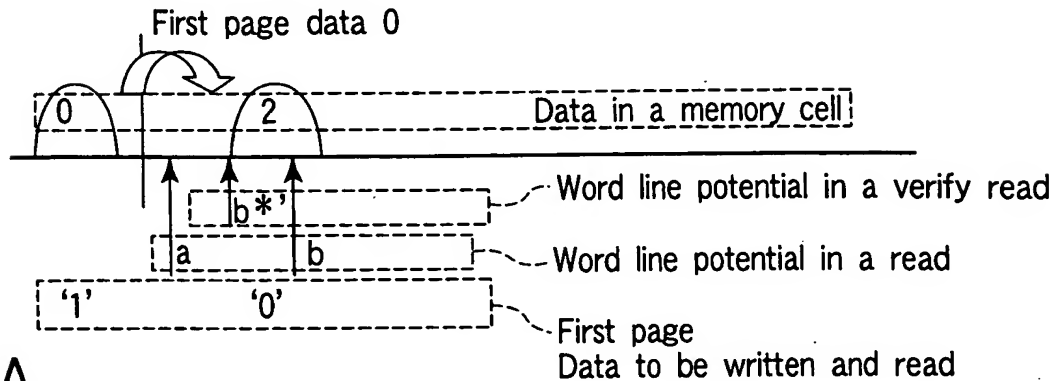


FIG. 1A

Before writing the second page and after writing the adjacent cells

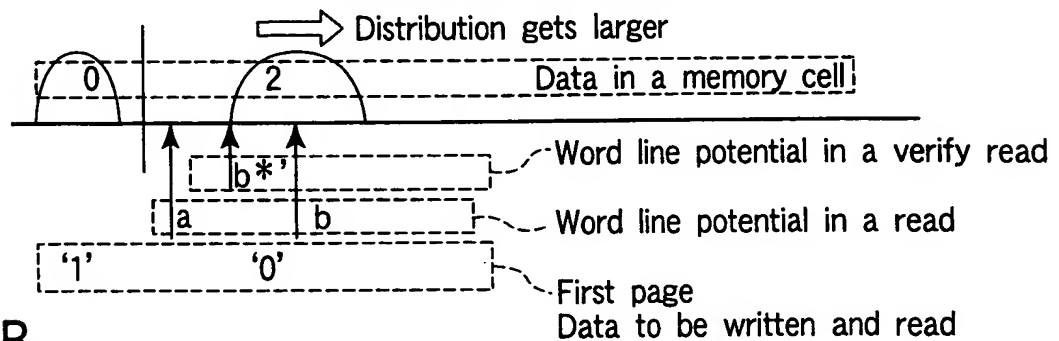


FIG. 1B

After writing the second page

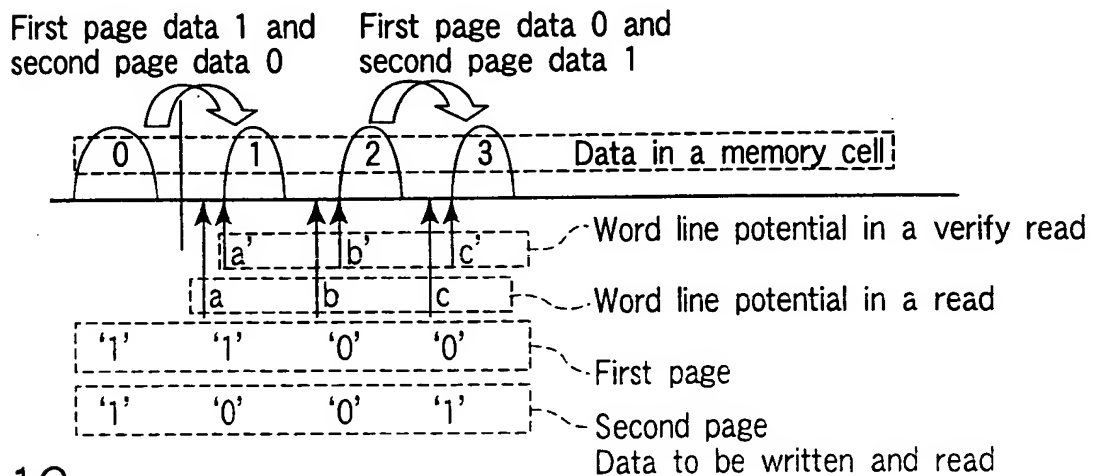


FIG. 1C

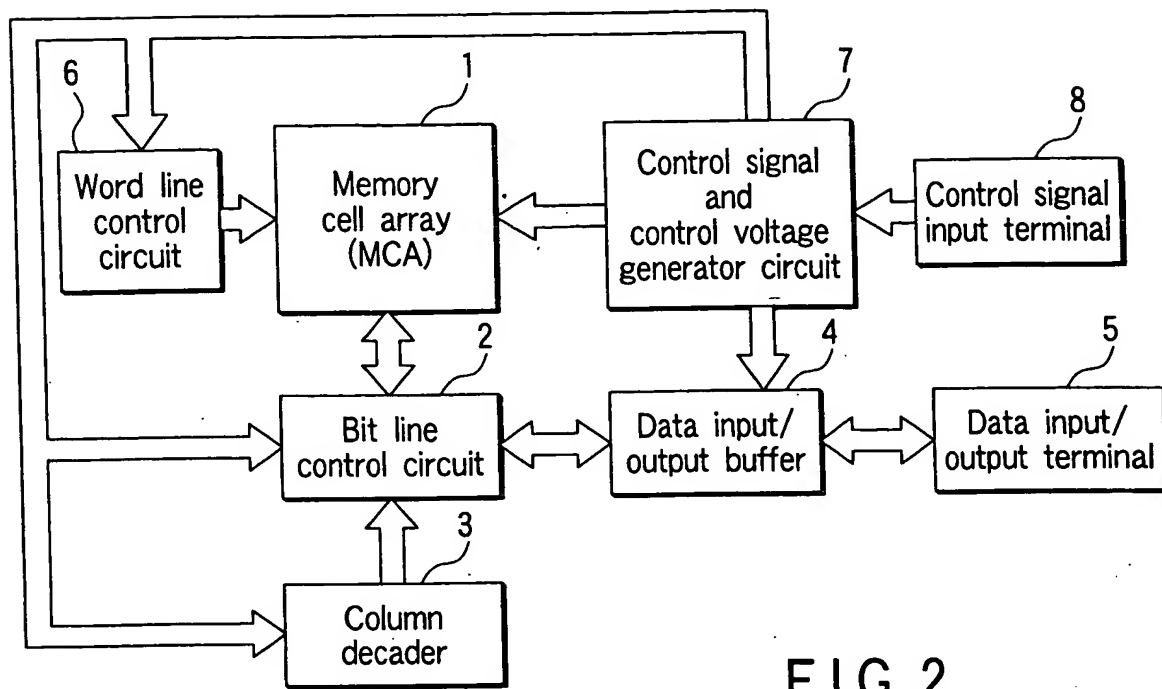


FIG. 2

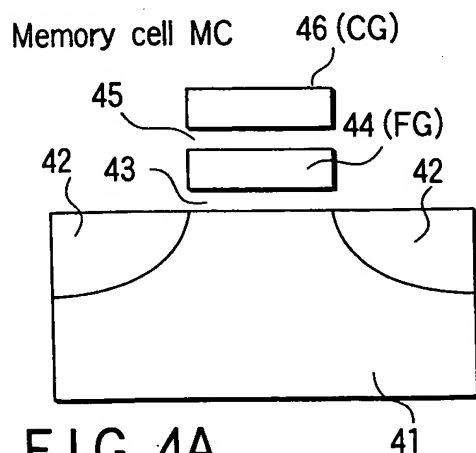


FIG. 4A

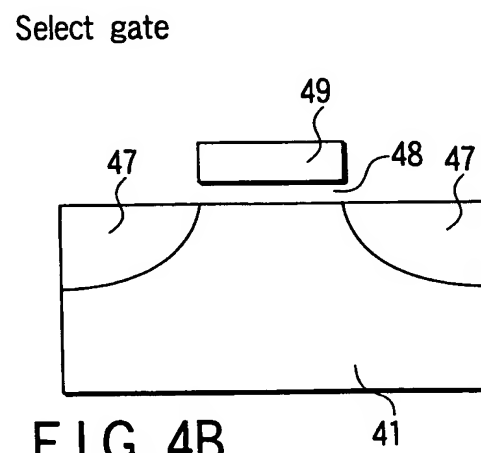


FIG. 4B

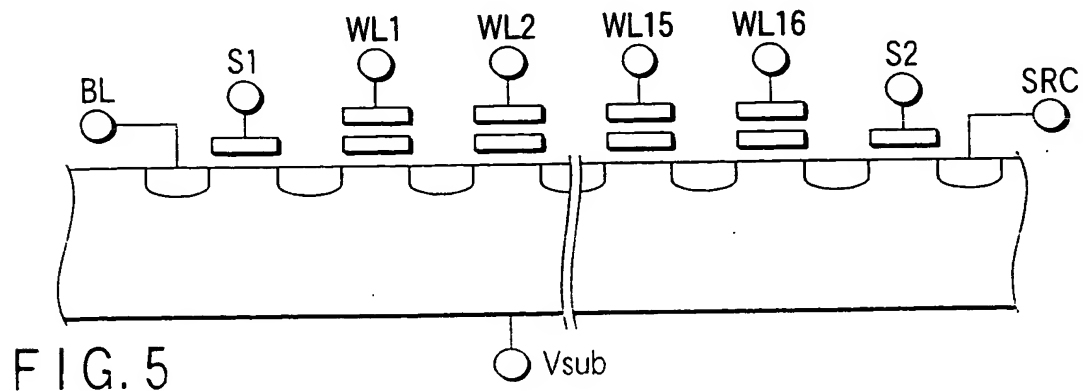
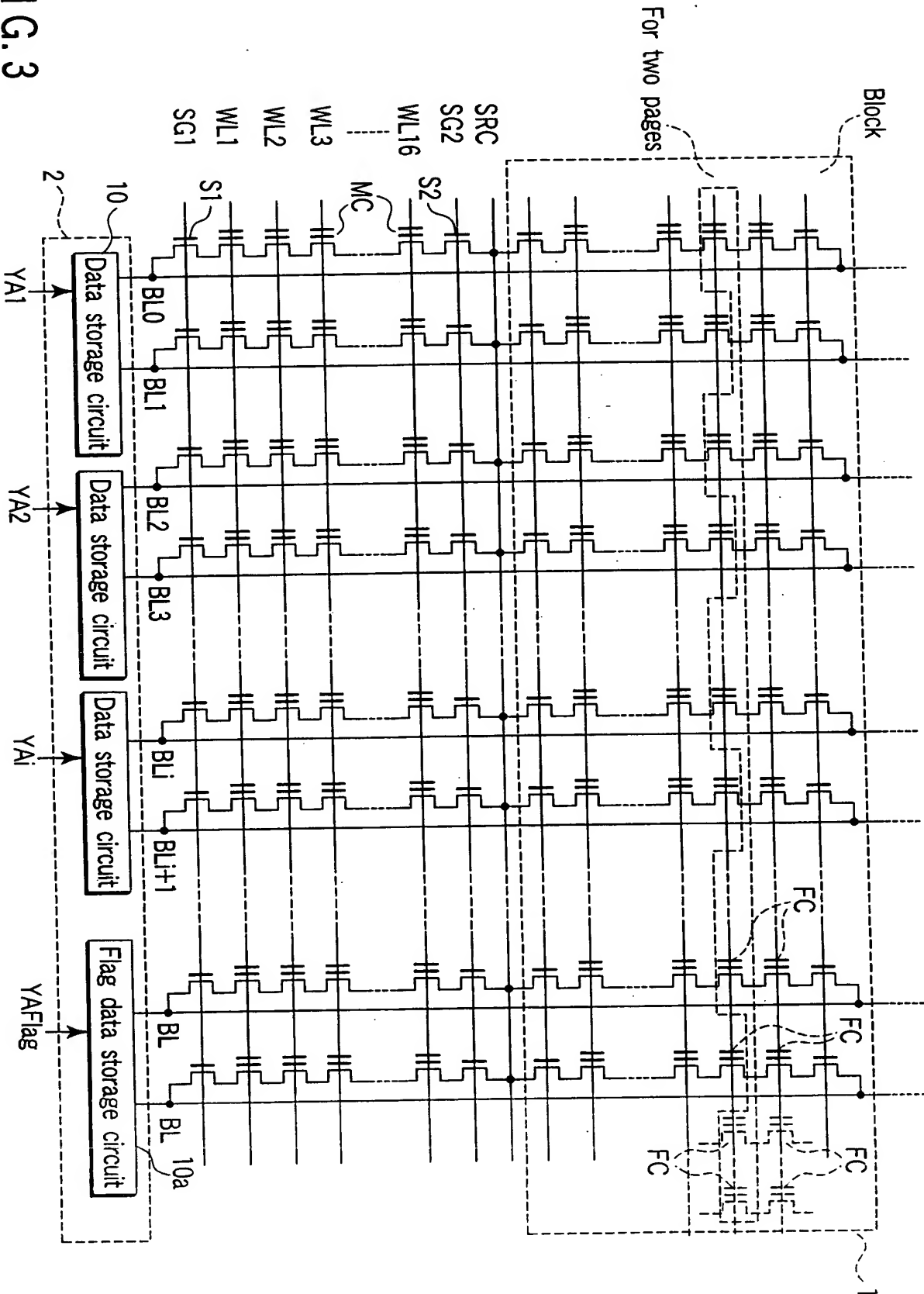
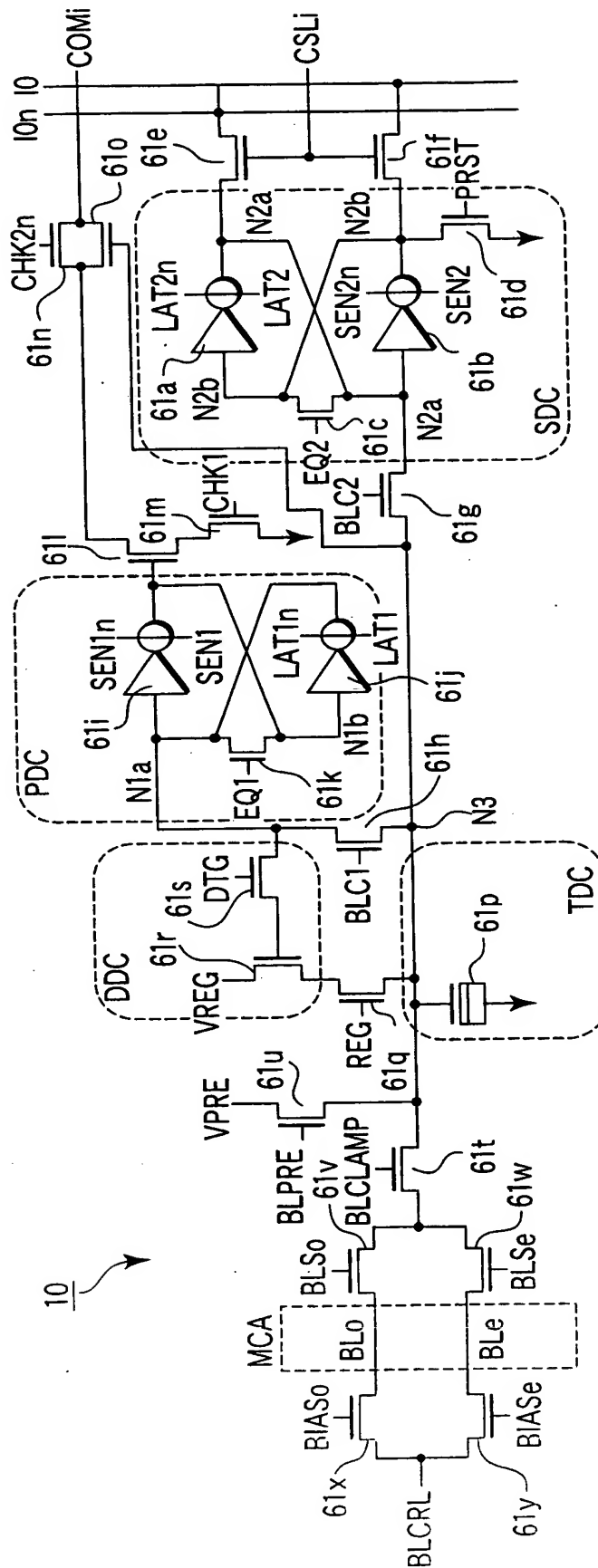


FIG. 5

FIG. 3





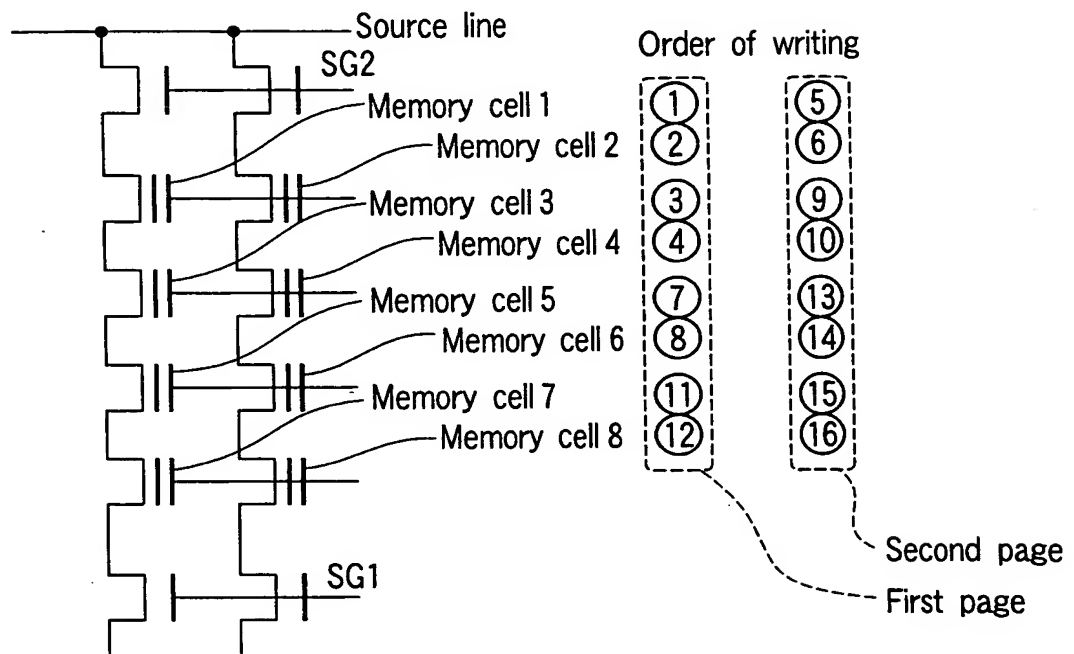


FIG. 7

Writing the first page

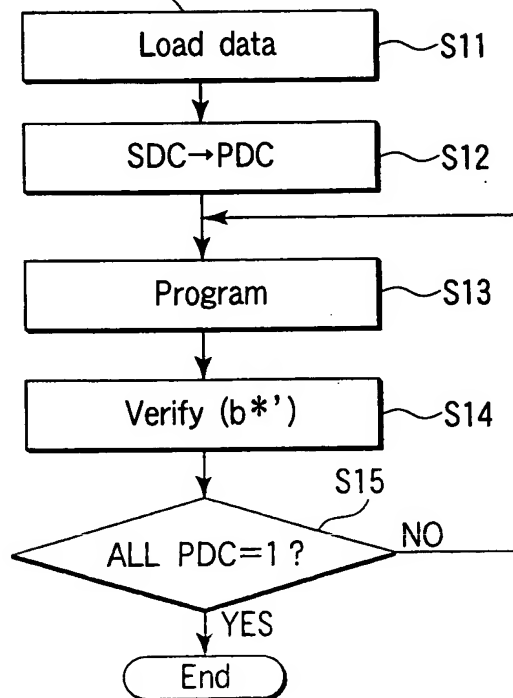


FIG. 8

Writing the second page

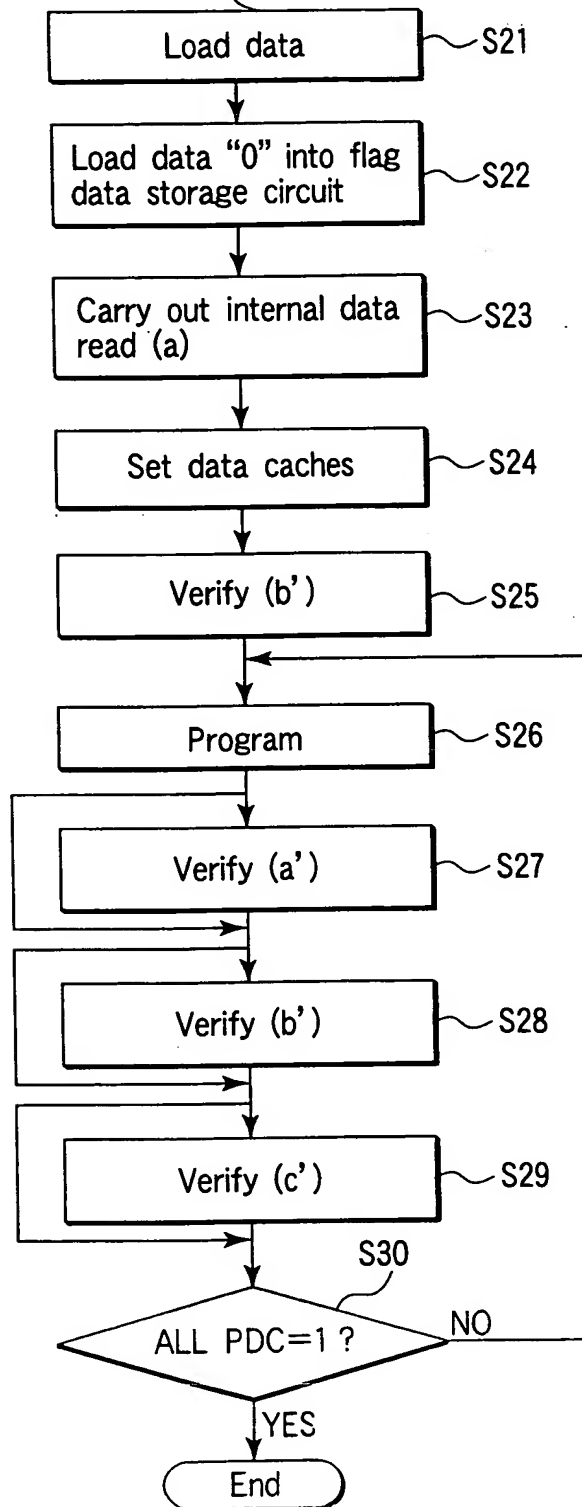


FIG. 9

After data load and internal read

	Data in memory cell after writing				
	0	1	2	3	
SDC	1	0	0	1	Data to be written and read inputted from the outside world
PDC	0	0	1	1	Data read by internal read

FIG. 10A

After setting data caches

	Data in memory cell after writing				
	0	1	2	3	
SDC	1	1	0	0	Used for charging in verifying memory cell data 1
DDC	0	1	1	0	Used for charging in verifying memory cell data 2
PDC	1	0	0	0	1 : Write unselected 0 : Write

FIG. 10B

Data cache setting procedure

SDC				DDC				PDC				TDC				Data in memory cell after writing
0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	
1	0	0	1					0	0	1	1					After internal data read
1	0	0	1	0	0	1	1	0	0	1	1					Copy data in PDC into DDC
1	0	0	1	0	0	1	1	1	0	0	1					Copy data in SDC into PDC
1	0	0	1	0	0	1	1	1	0	0	0	1	1	1	1	TDC=H
1	0	0	1	0	0	1	1	1	0	0	1	1	1	0	0	VREG=L, REG=H
1	1	0	0	0	0	1	1	1	0	0	1	1	1	0	0	Copy data in TDC into SDC
1	1	0	0	0	0	1	1	1	0	0	1	1	0	0	1	Copy data in PDC into TDC
1	1	0	0	0	0	1	1	1	0	0	1	1	0	0	0	VREG=L, REG=H
1	1	0	0	1	0	0	1	1	0	0	1	1	0	0	0	Copy data in PDC into DDC
1	1	0	0	1	0	0	1	1	0	0	0	1	0	0	0	Copy data in TDC into PDC

FIG.11

1	1	0	0	1	0	0	1	0	0	1	0	0	0	1	1	1	1	TDC=H
1	1	0	0	1	0	0	1	0	0	1	0	0	0	0	1	1	0	VREG=L, REG=H
1	1	0	0	1	0	0	1	0	0	1	0	0	0	0	1	1	0	Copy data in PDC into DDC
1	1	0	0	1	0	0	1	0	0	0	1	1	0	0	1	1	0	Copy data in TDC into PDC
1	1	0	0	1	0	0	1	0	0	0	1	1	0	0	0	0	0	TDC=L
1	1	0	0	1	0	0	1	0	0	0	1	1	0	1	0	0	0	VREG=H, REG=H
1	1	0	0	1	0	1	0	1	1	0	1	1	0	1	0	0	0	Copy data in PDC into DDC
1	1	0	0	1	0	0	1	1	0	0	1	0	0	1	0	0	0	Copy data in TDC into PDC
SDC				DDC				PDC				TPC						

FIG.12

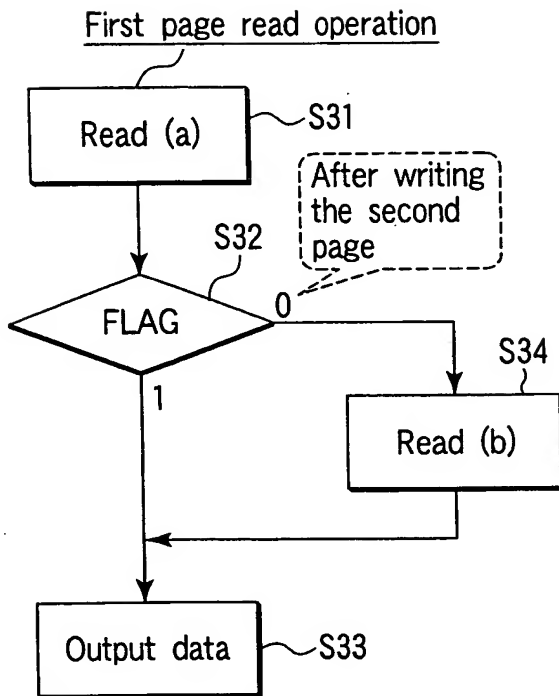


FIG. 13

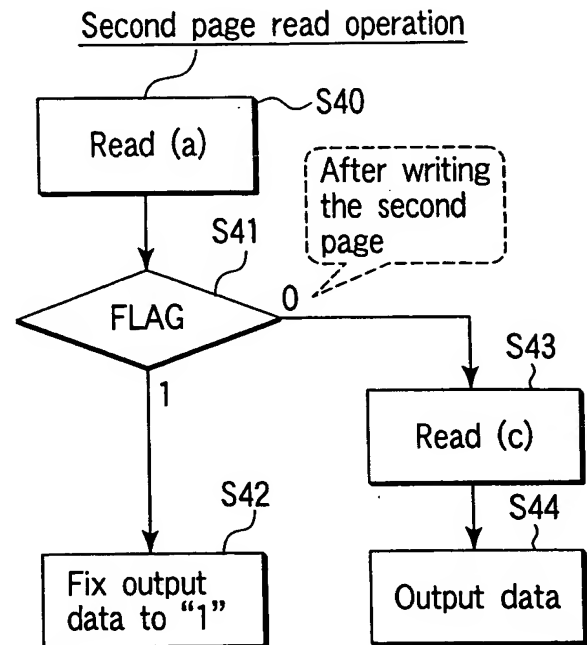


FIG. 15

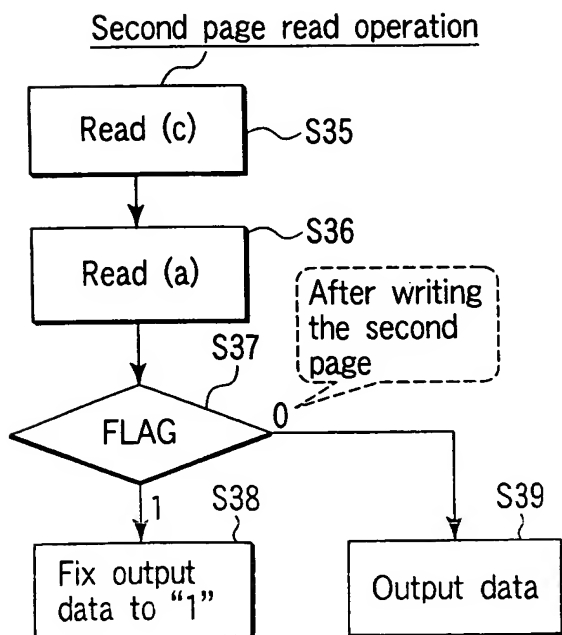


FIG. 14

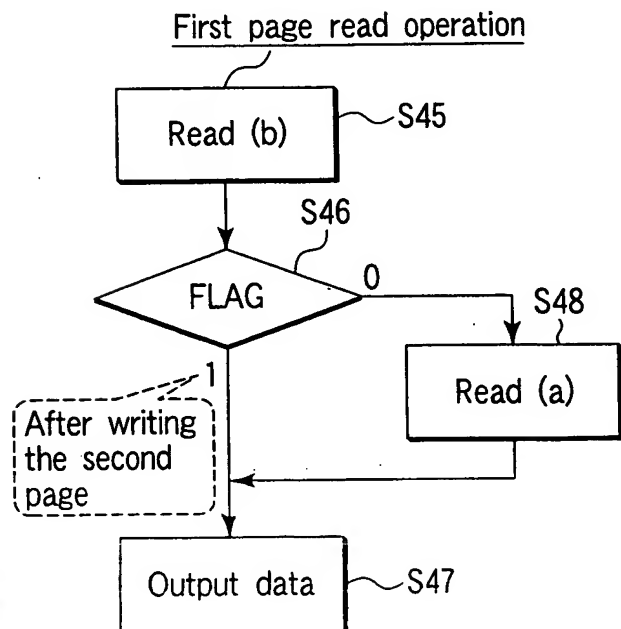


FIG. 16

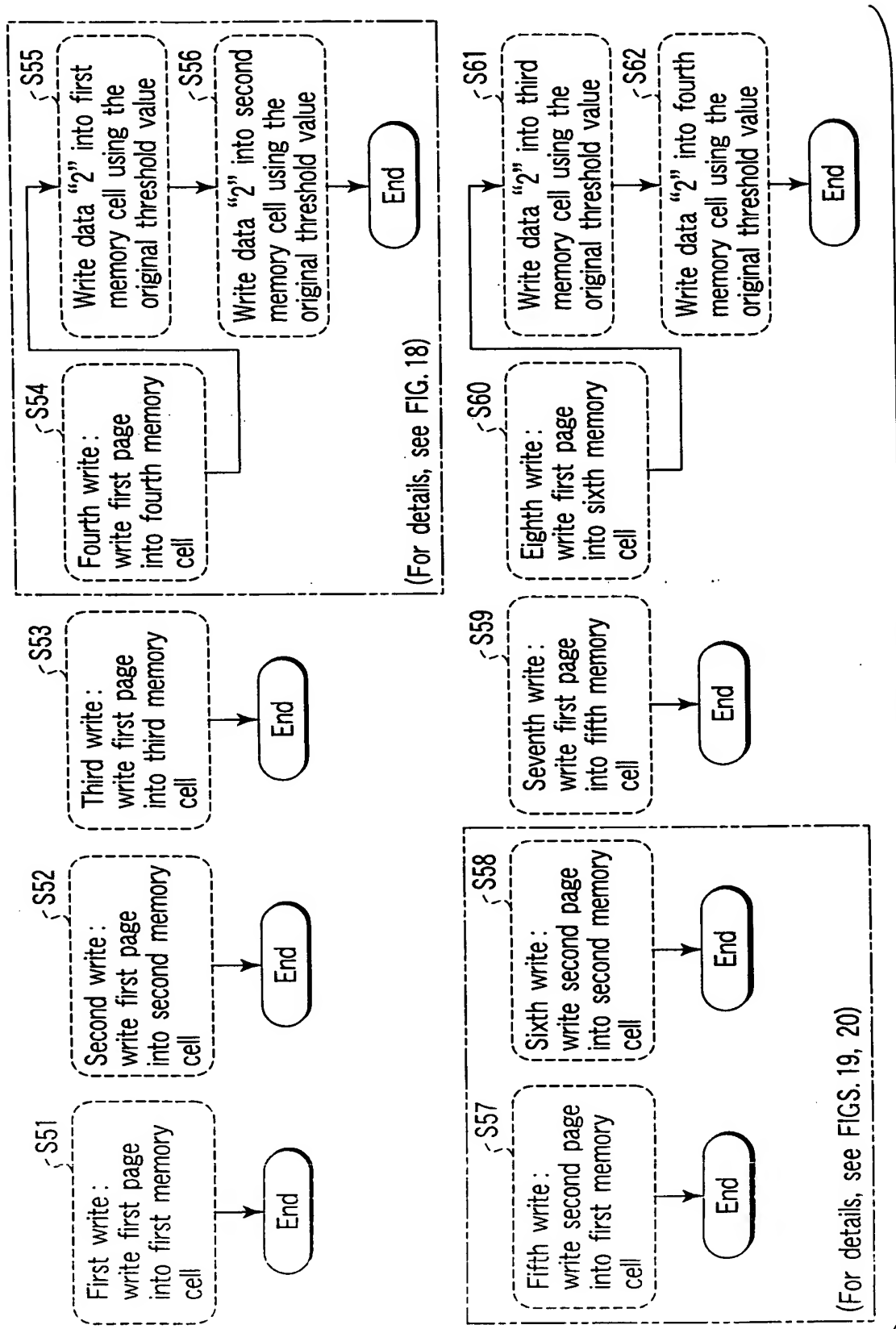


FIG. 17

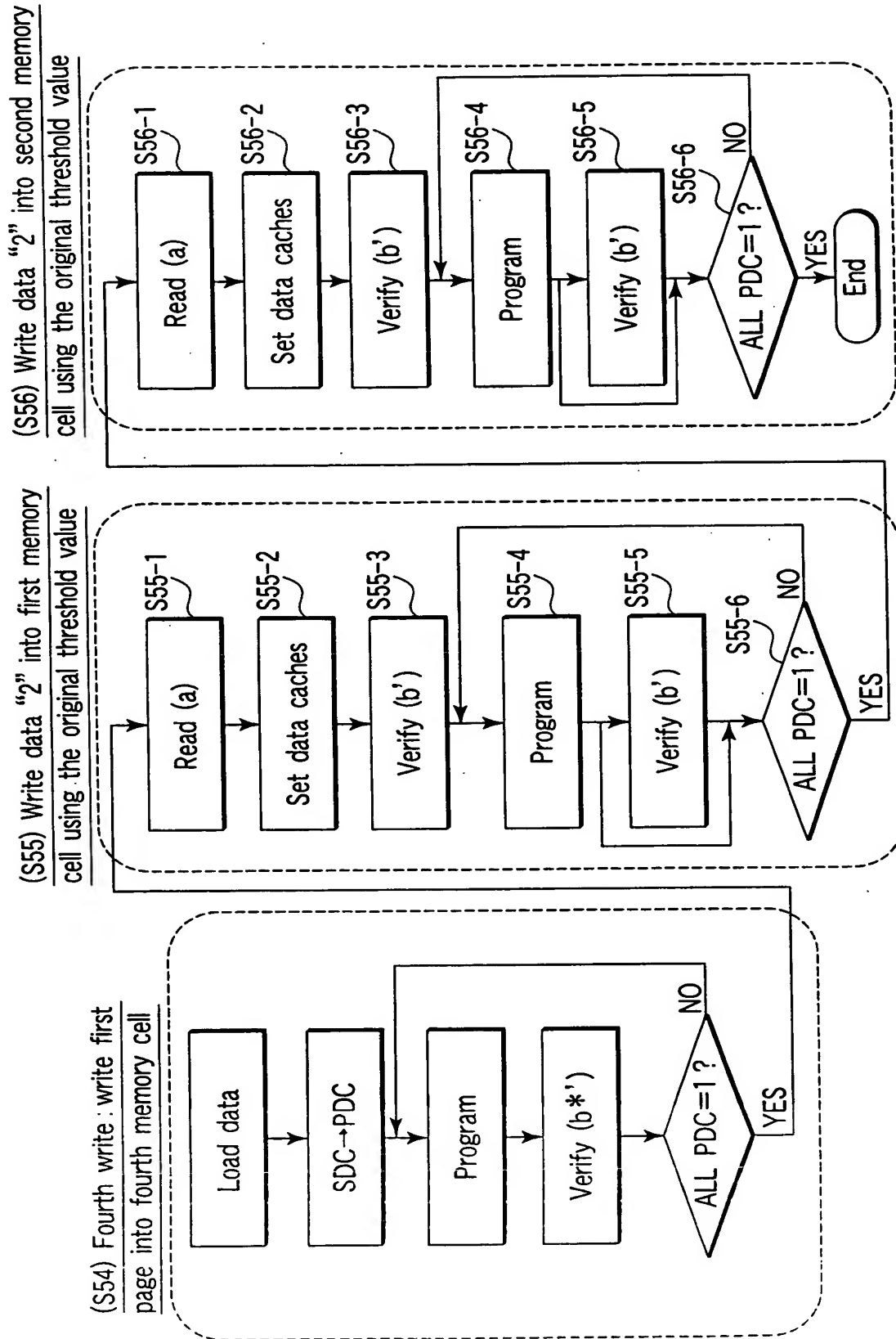


FIG. 18

(S57) Fifth write : write second
page into first memory cell

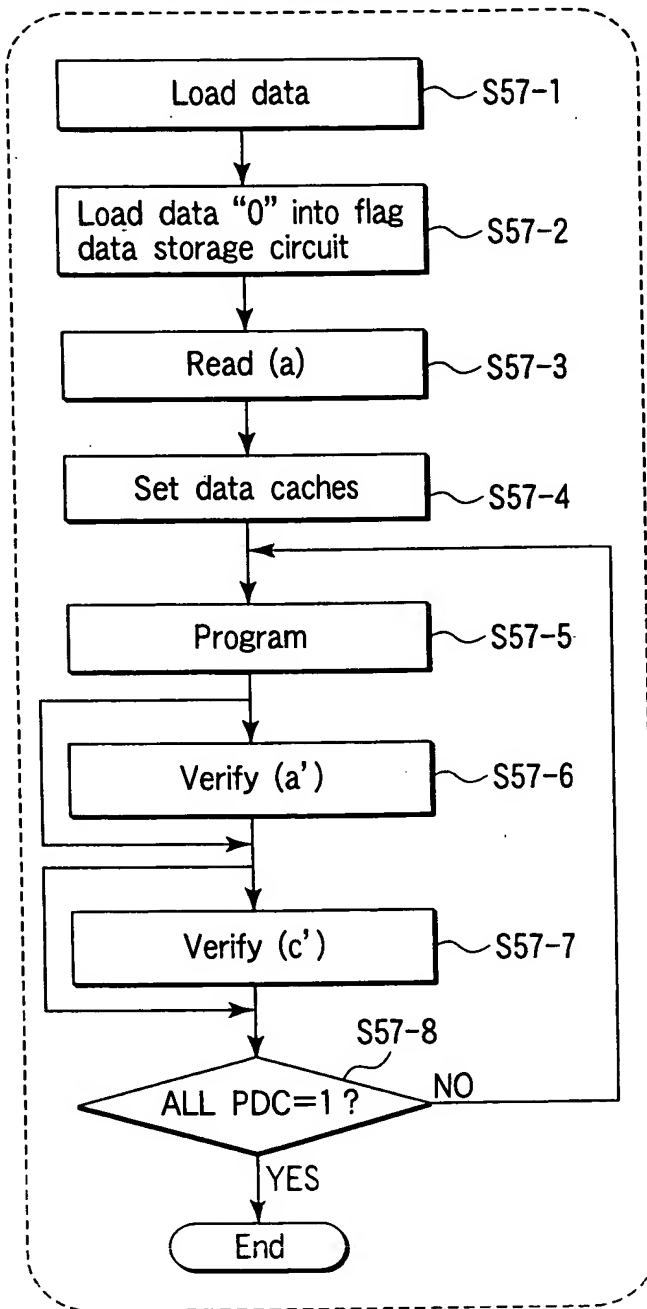


FIG. 19

(S58) Sixth write : write second
page into second memory cell

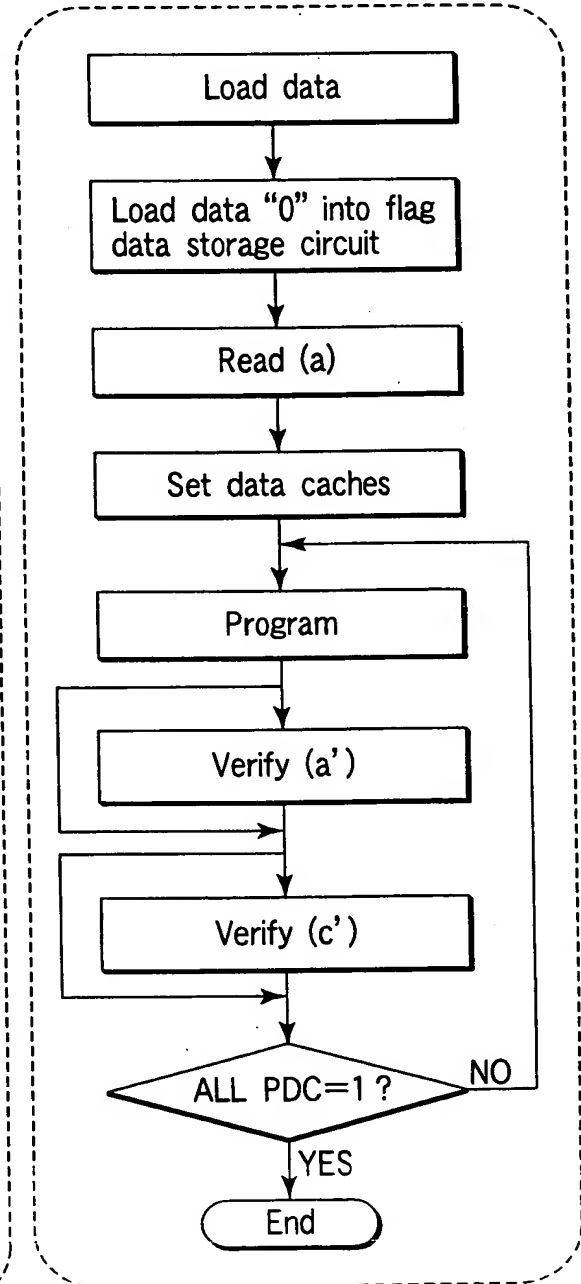
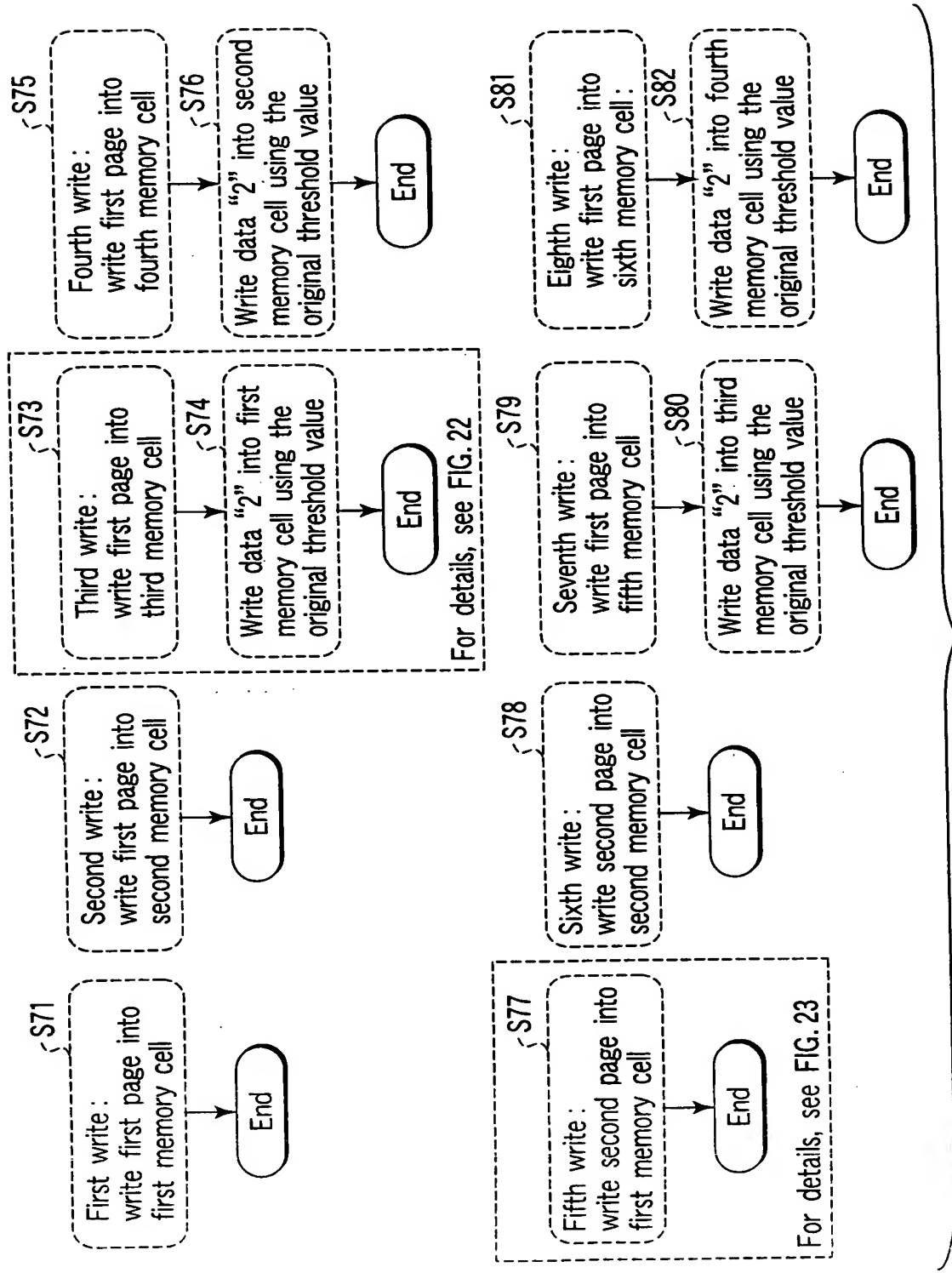
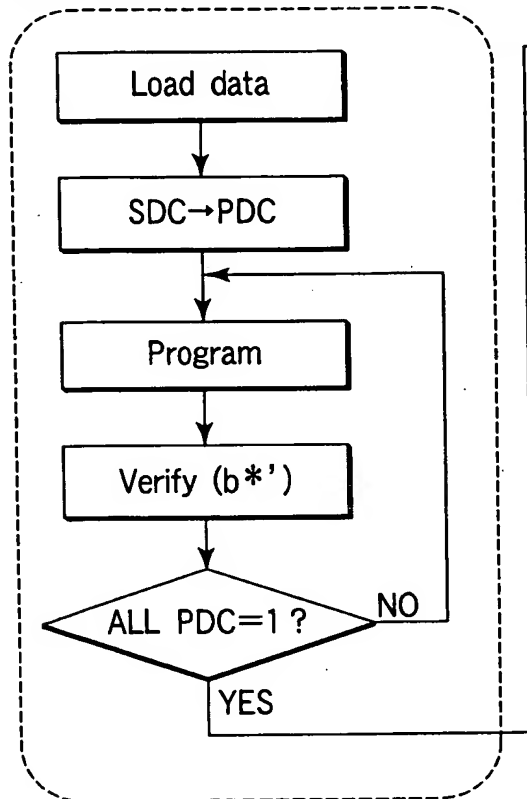


FIG. 20



(S73) Third write : write first
page into third memory cell



(S74) Write data "2" into first memory
cell using the original threshold value

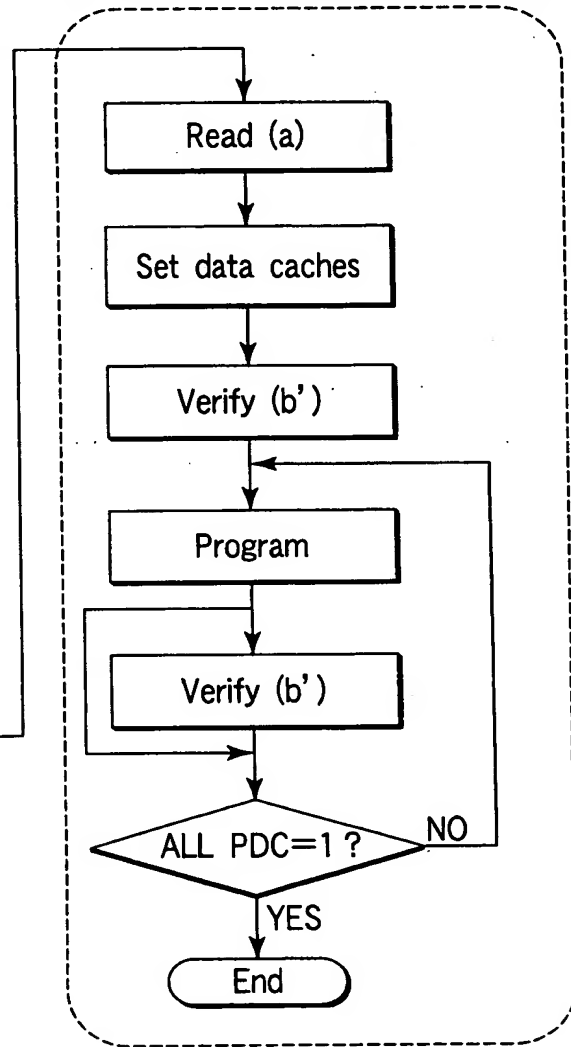


FIG. 22

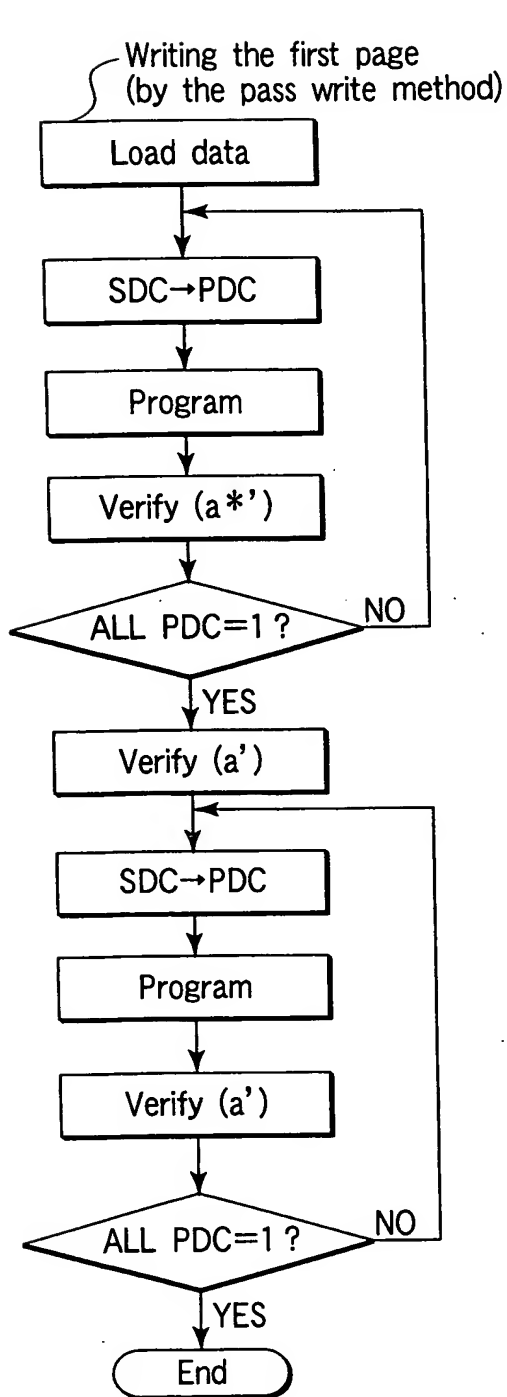


FIG. 23A

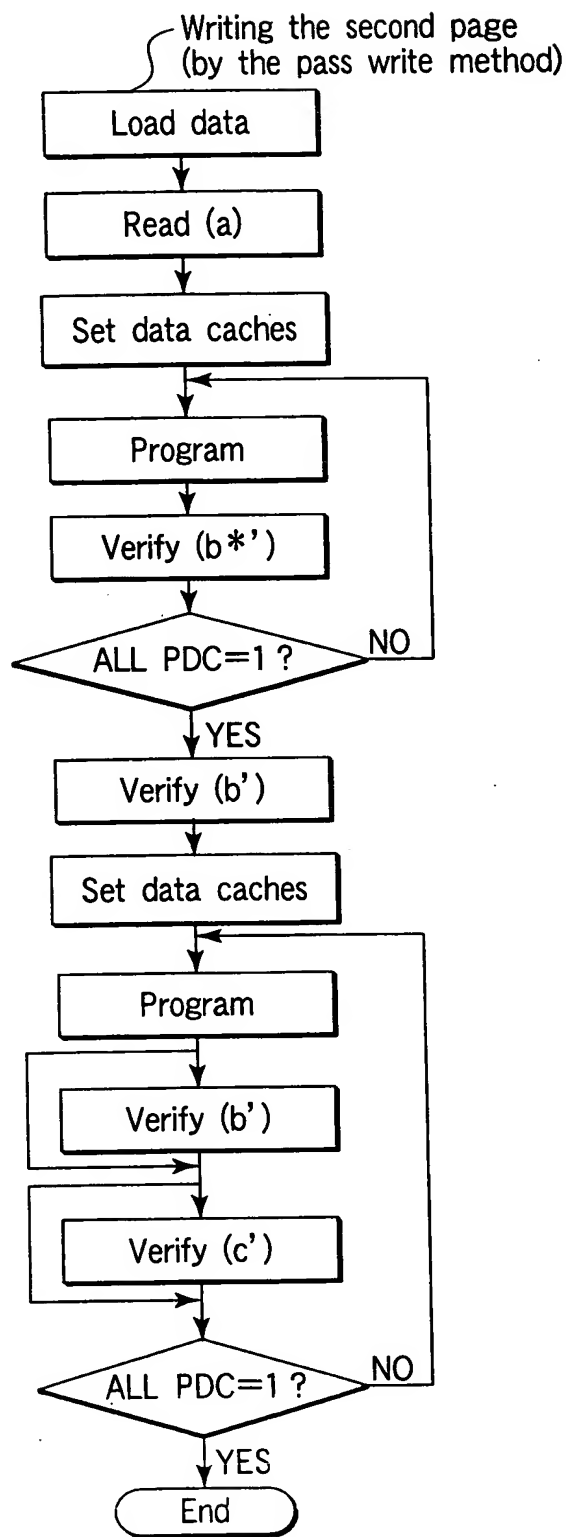


FIG. 23B

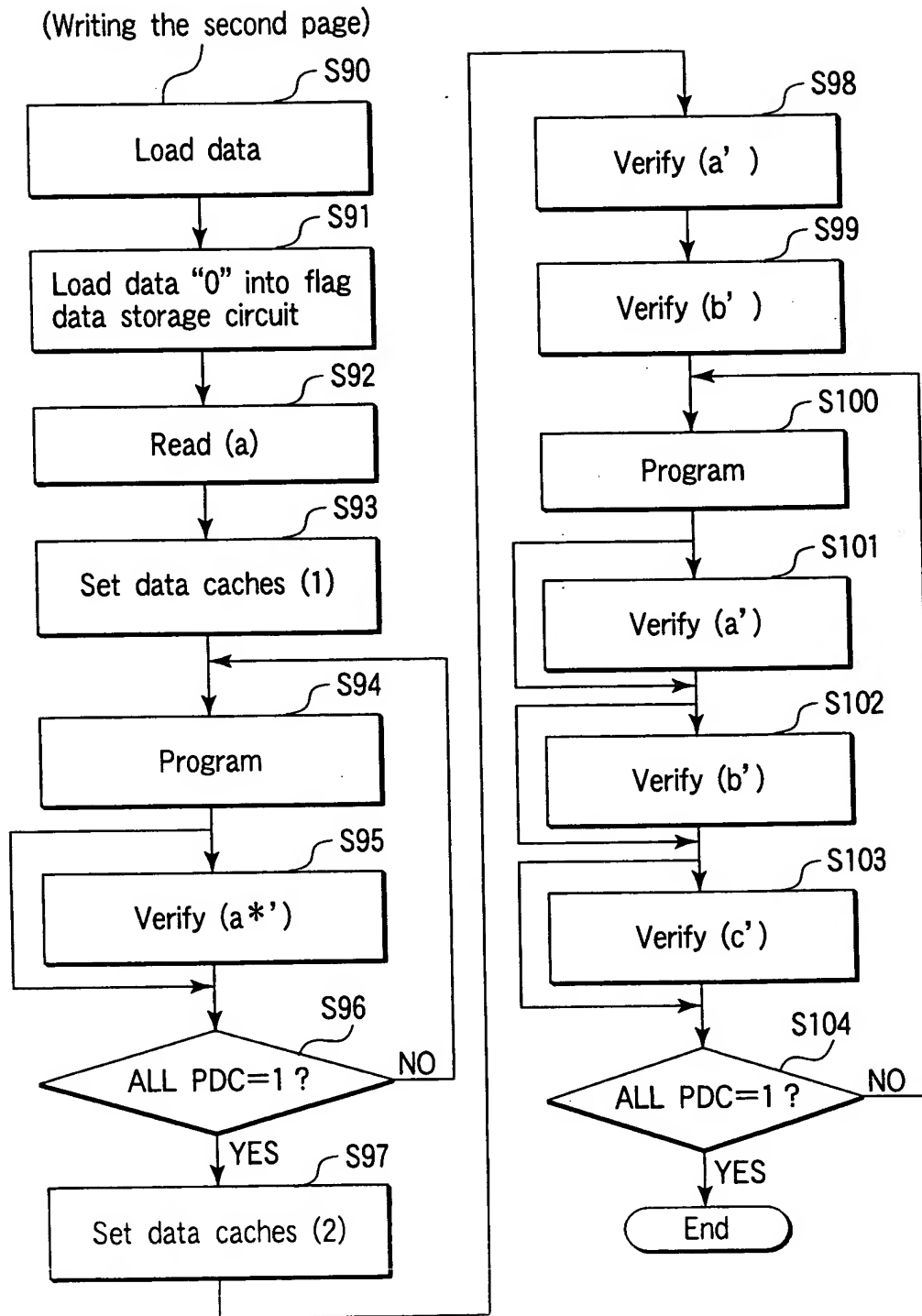


FIG. 24

Data cache setting 1

	Data in memory cell after writing				
	0	1	2	3	
SDC	1	0	0	1	
DDC	0	0	1	1	
PDC	1	0	1	1	1: Write unselected 0: Write

FIG. 25

(Writing the second page)

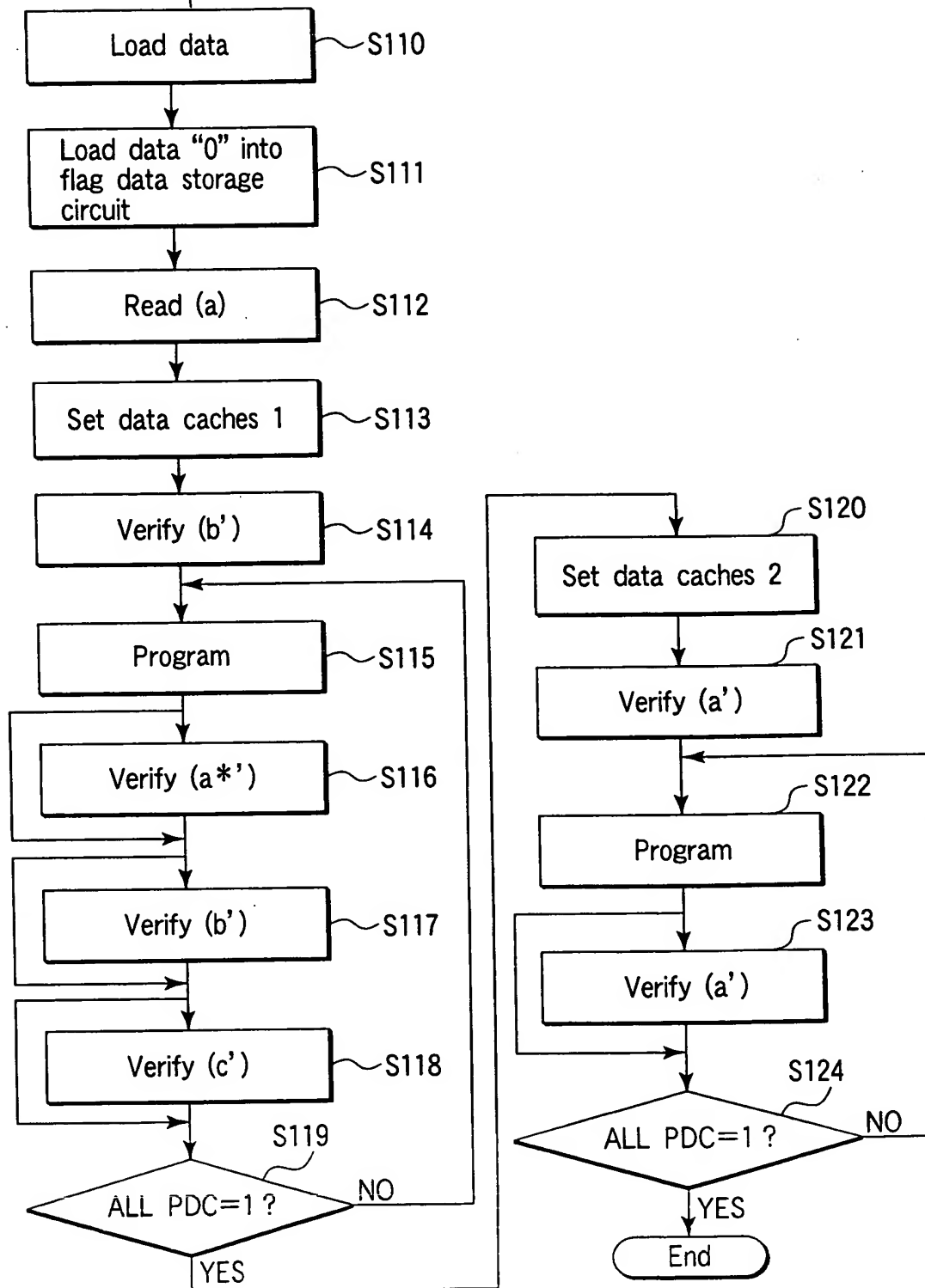


FIG. 26

Data cache setting 1

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	0	0	Used for charging in verifying memory cell data 1
DDC	0	1	1	0	Used for charging in verifying memory cell data 2
PDC	1	0	0	0	1 : Write unselected 0 : Write

FIG. 27A

Data cache setting 2

	Data in memory cell after writing				
	0	1	2	3	
PDC	1	0	1	1	1 : Write unselected 0 : Write

FIG. 27B

(Writing the second page)

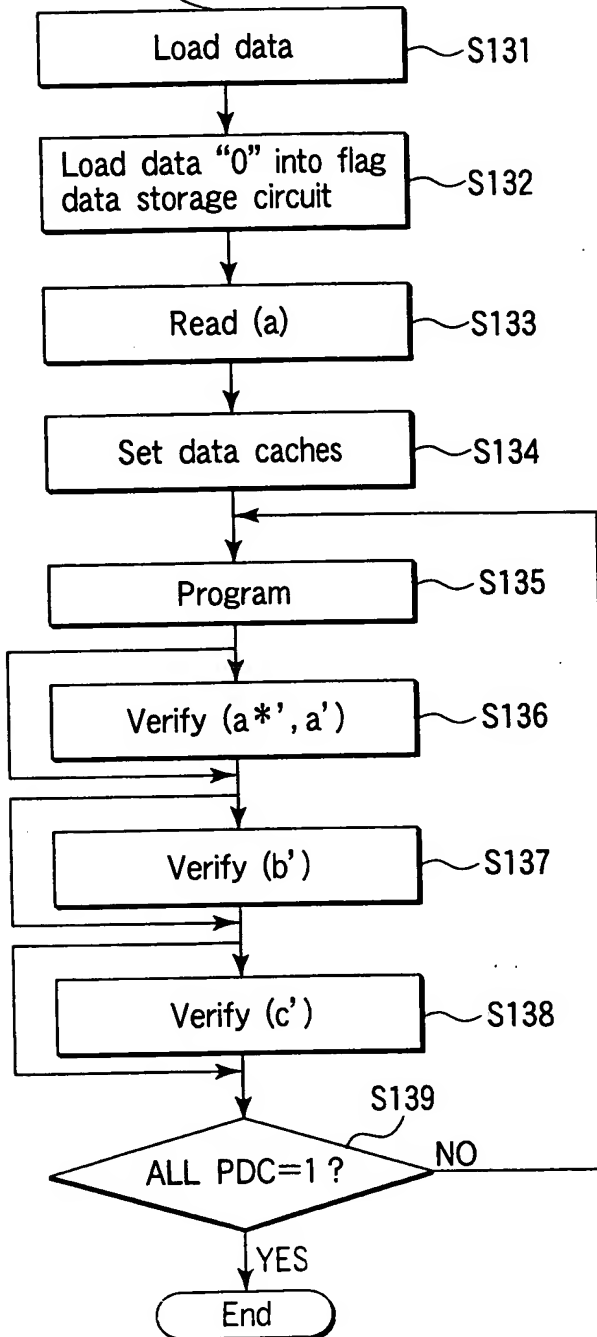


FIG. 28

After data load and internal read

	Data in memory cell after writing				
	0	1	2	3	
SDC	1	0	0	1	Data to be written and read inputted from the outside world
PDC	0	0	1	1	Data read by internal read

FIG. 29A

After data cache setting

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	1	0	Used for charging in verifying memory cell data 2
DDC	1	0	1	1	Used for precharging bit line in programming and for charging in verifying memory cell data 1
PDC	1	0/1	0	0	1 : Write unselected 0 : Write

FIG. 29B

Precharge bit line on the basis of the data in DDC

	Data in memory cell after writing			
	0	1	2	3
Bit line	Vdd	F (Vss)	Vdd	Vdd

FIG. 30A

With BLC1 = Vclamp, connect PDC to bit line

	Data in memory cell after writing				
	0	1	2	3	
Bit line	Vdd	0/Inter-mediate	0	0	

FIG. 30B

During program recovery, transfer data in PDC to DCC, invent data in DDC, and transfer the inverted data to PDC

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	1	0	Used for charging in verifying memory cell data 2
DDC	1	0/1	0	0	1 : Write unselected 0 : Write
PDC	0	1	0	0	Used for precharging bit line in programming and for charging in verifying memory cell data 1

FIG. 30C

Verify (a)
 Charge bit line on the basis of data in PDC
 Discharge bit line at a potential of $WL = a^*$
 Invert data in PDC while discharging bit line

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	1	0	Used for charging in verifying memory cell data 2
DDC	1	0/1	0	0	1: Write unselected 0: Write
PDC	1	0	1	1	Used for precharging bit line in programming and for charging in verifying memory cell data 1

FIG. 31A

Load the potential of bit line into TDC
 With $V_{REG} = H$ and $REG = H$, make TDC 1 when dynamic data is 1
 Transfer data in PDC to DDC and data in TDC to PDC

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	1	0	Used for charging in verifying memory cell data 2
DDC	1	0	0	1	User for precharging bit line in programming and for charging in verifying memory cell data 1
PDC	1	0/1	1	1	1: Write unselected 0: Write

FIG. 31B

With WL = a', discharge bit line
 With VREG = H and REG = H, set 1 in TDC when dynamic data is 1
 Transfer data in PDC to DDC
 Transfer data in TDC to PDC

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	1	0	Used for charging in verifying memory cell data 2
DDC	1	0/1	0	0	1: Write unselected 0: Write
PDC	1	0	1	1	Used for precharging bit line in programming and for charging in verifying memory cell data 1

FIG. 32A

Transfer data in DDC to PDC
 Then, transfer data in PDC to DDC

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	1	0	Used for charging in verifying memory cell data 2
DDC	1	0	1	1	Used for precharging bit line in programming and for charging in verifying memory cell data 1
PDC	1	0/1	0	0	1: Write unselected 0: Write

FIG. 32B

With memory cell data 1, all of the writing with verify (a*) is completed
 (the writing with verify (a') might not be completed)

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	1	0	Used for charging in verifying memory cell data 2
DDC	1	0	1	1	Used for precharging bit line in programming and for charging in verifying memory cell data 1
PDC	1	1	0	0	1 : Write unselected 0 : Write

FIG. 33A

With memory cell data 1, all of the writing with verify (a') is completed
 (the writing with verify (a*) might not be completed)

	Data in memory cell after writing				
	0	1	2	3	
SDC	0	1	1	0	Used for charging in verifying memory cell data 2
DDC	1	1	1	1	Used for precharging bit line in programming and for charging in verifying memory cell data 1
PDC	1	1	0	0	1 : Write unselected 0 : Write

FIG. 33B

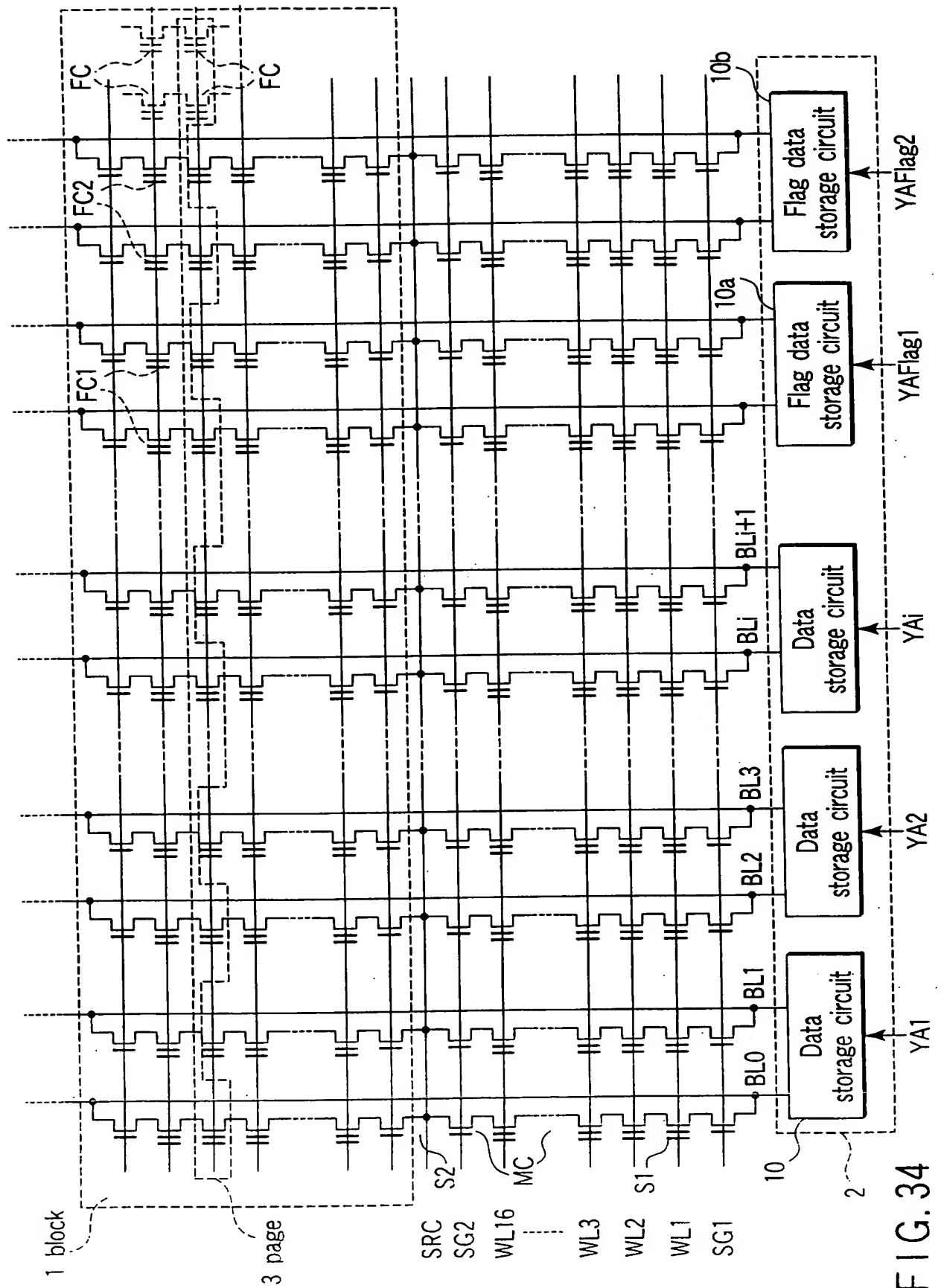


FIG. 34

(After writing first page and before writing second page)

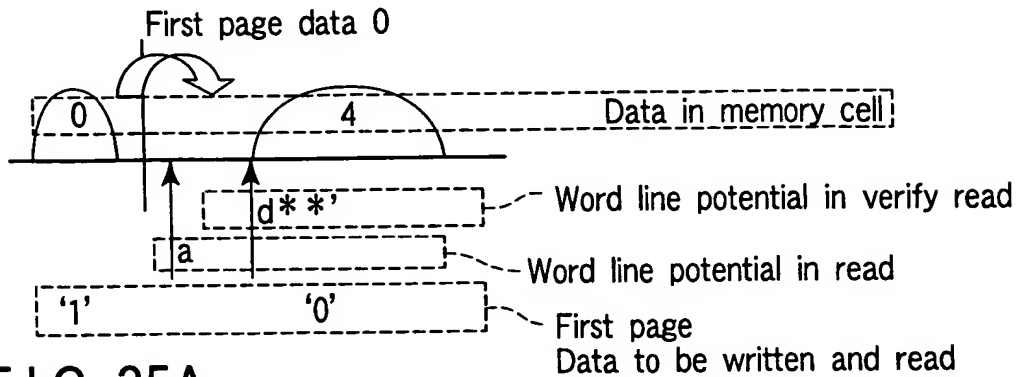


FIG. 35A

(After writing first page, before writing second page,
 and after writing adjacent cells of first page)

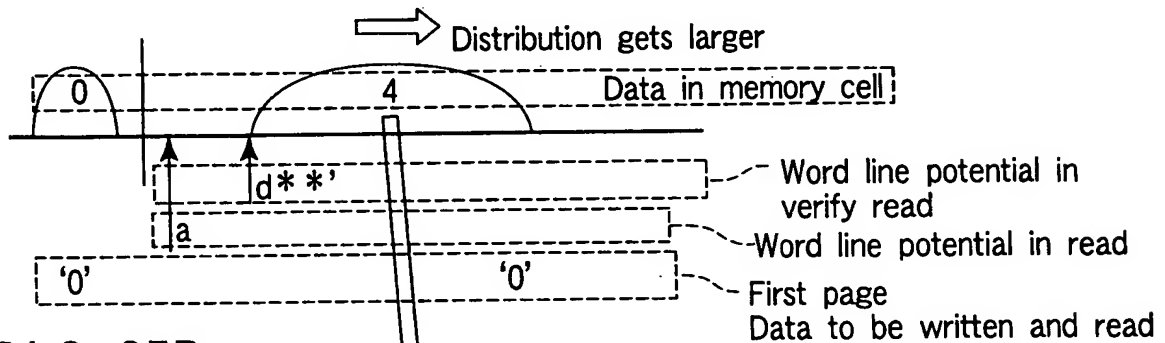


FIG. 35B

After writing second page, before writing third page,
 and after writing adjacent cells of second page

With first page data 1,
 second page data 0 is
 obtained

With first page data 0,
 second page data 1 is
 obtained

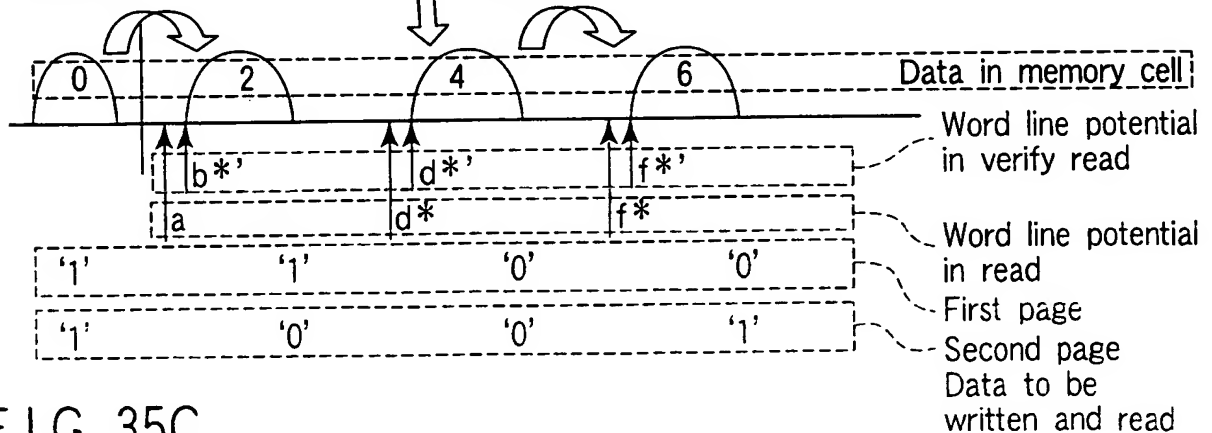


FIG. 35C

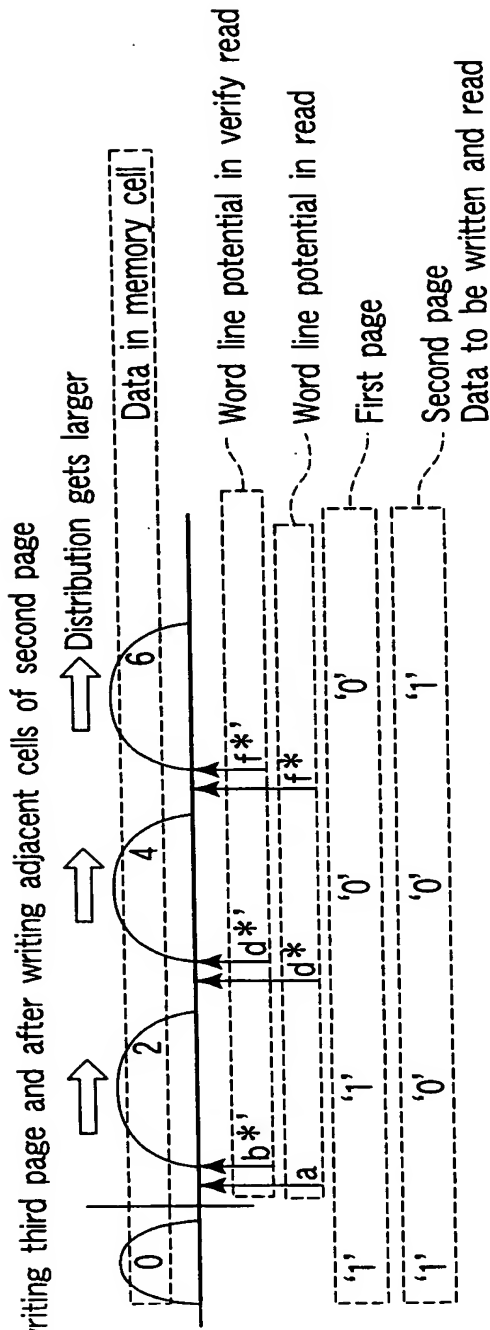


FIG. 36A

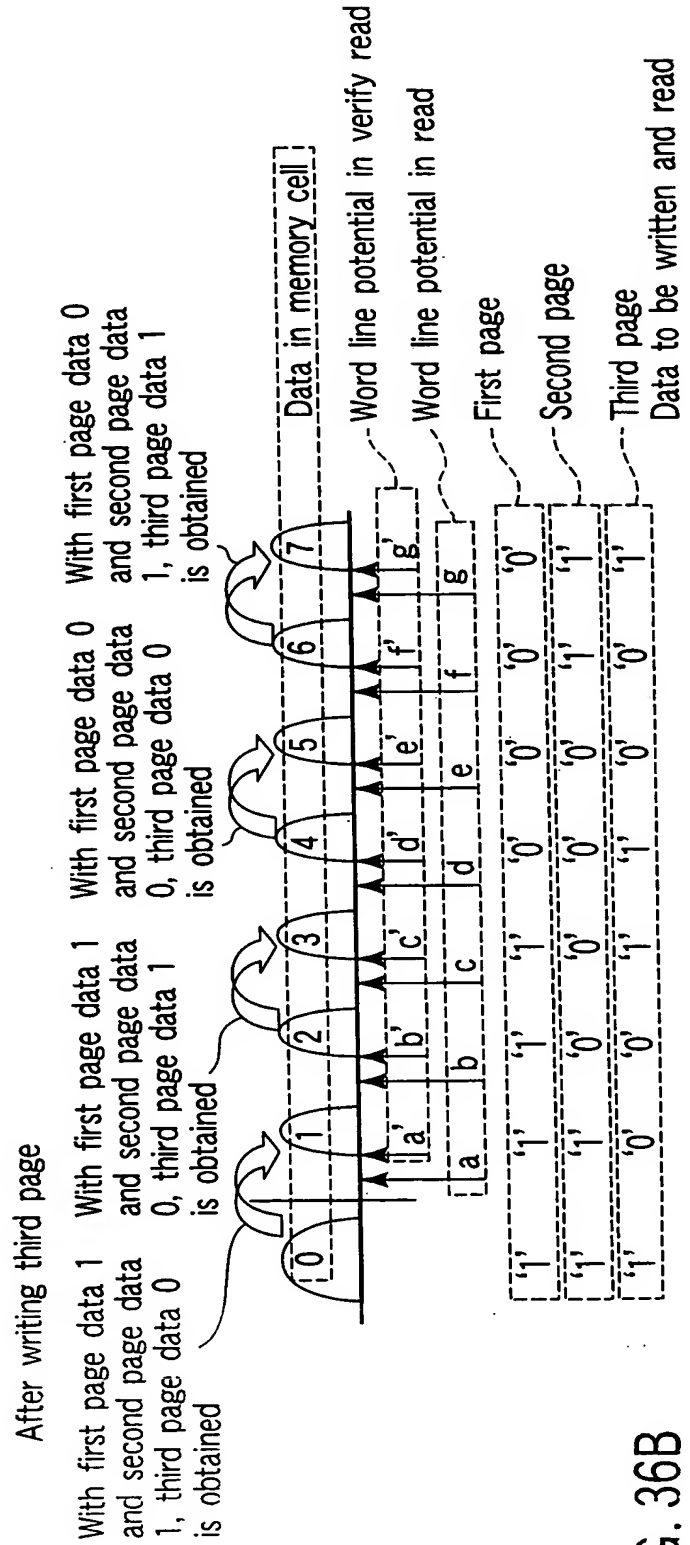


FIG. 36B

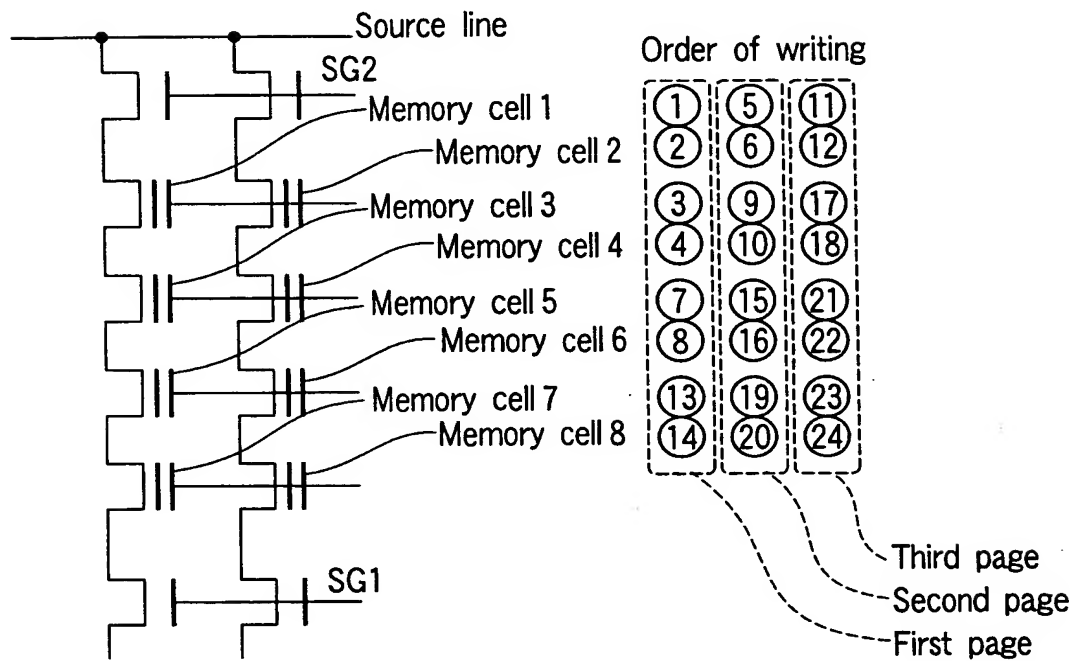


FIG. 37A

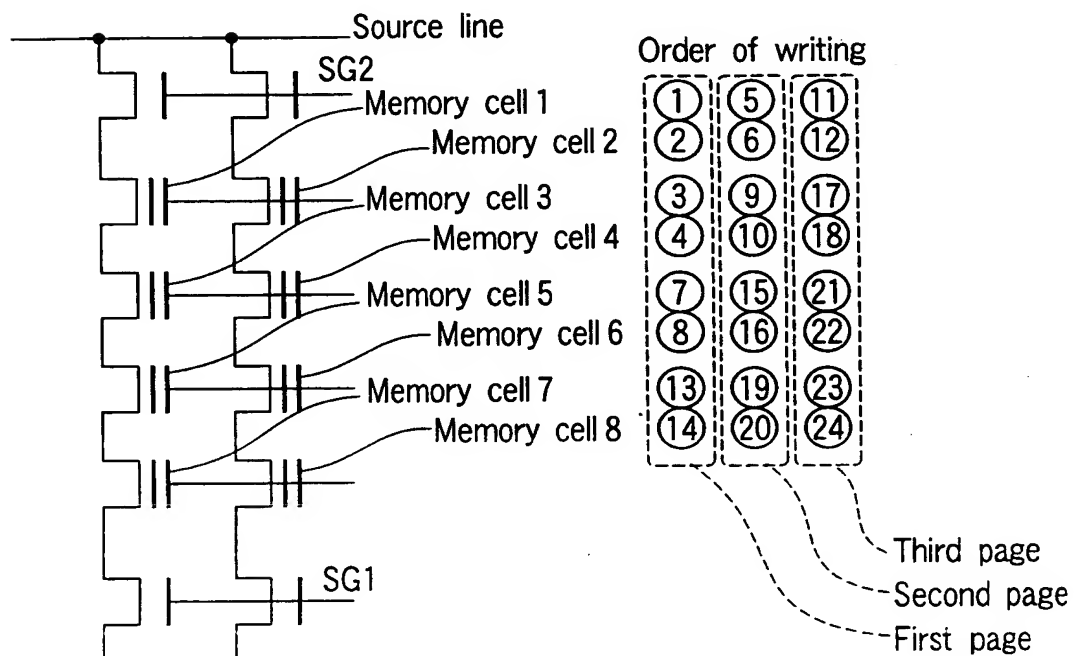


FIG. 37B

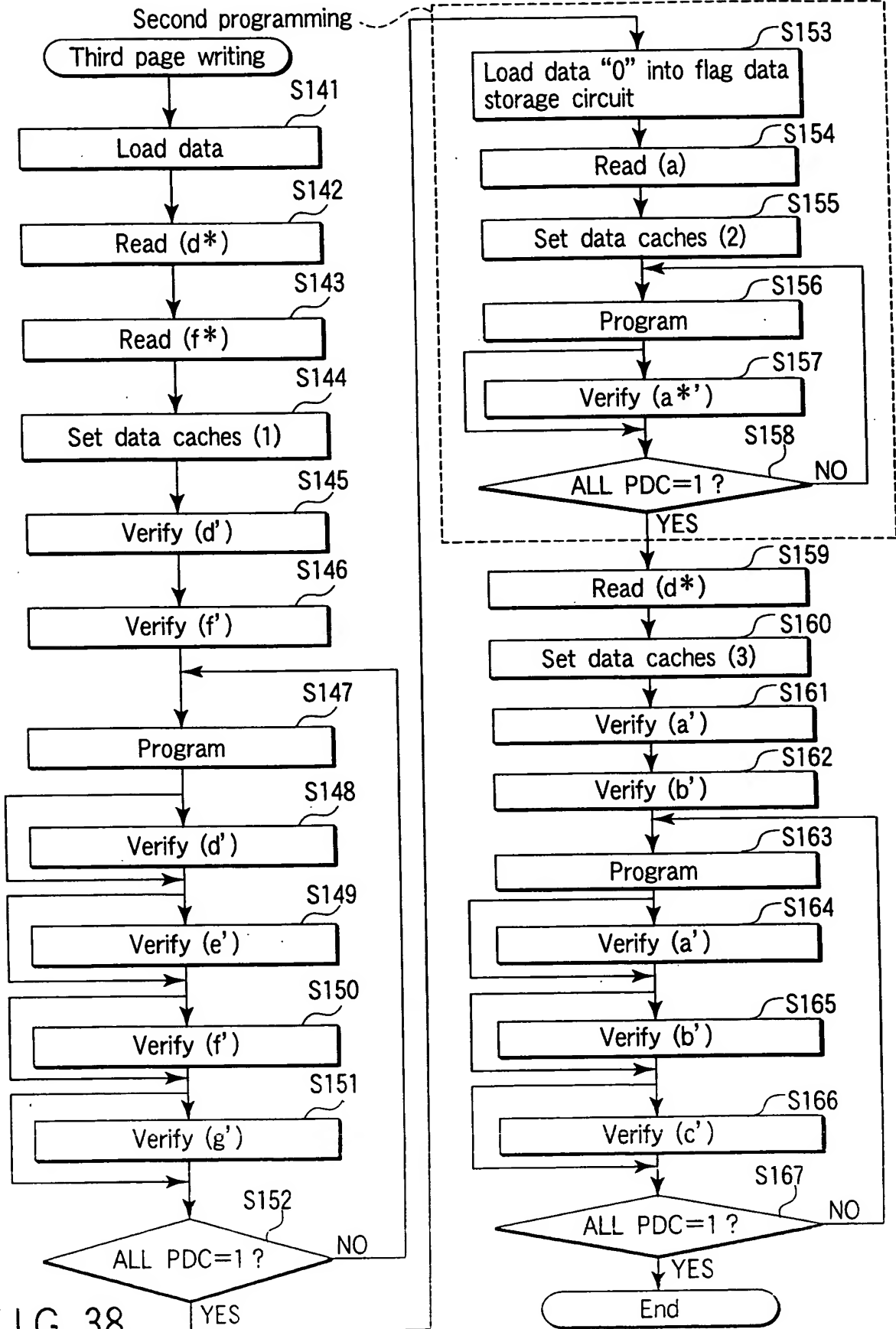


FIG. 38

After third page data load internal read 1

After third page data load internal read									
	Data in memory cell after writing								
	0	1	2	3	4	5	6		7
SDC	1	0	0	1	1	0	0	1	Data to be written and read inputted from the outside world
DDC	0	0	0	0	0	0	1	1	Data to be read by internal read
PDC	0	0	0	0	1	1	1	1	Data to be read by internal read

FIG. 39A

After third page data cache setting 1

After third page data cache setting 1									
	Data in memory cell after writing								
	0	1	2	3	4	5	6		7
SDC	1	1	1	1	1	1	0	0	Used far charging in verifying memory cell data items 5, 4
DDC	0	1	1	0	0	1	1	0	Used for charging in verifying memory cell data 6 Forced to be at VSS in verifying memory cell data 4
PDC	1	1	1	1	0	0	0	0	1 : Write unselected 0 : Write

FIG. 39B

After third page data cache setting 2

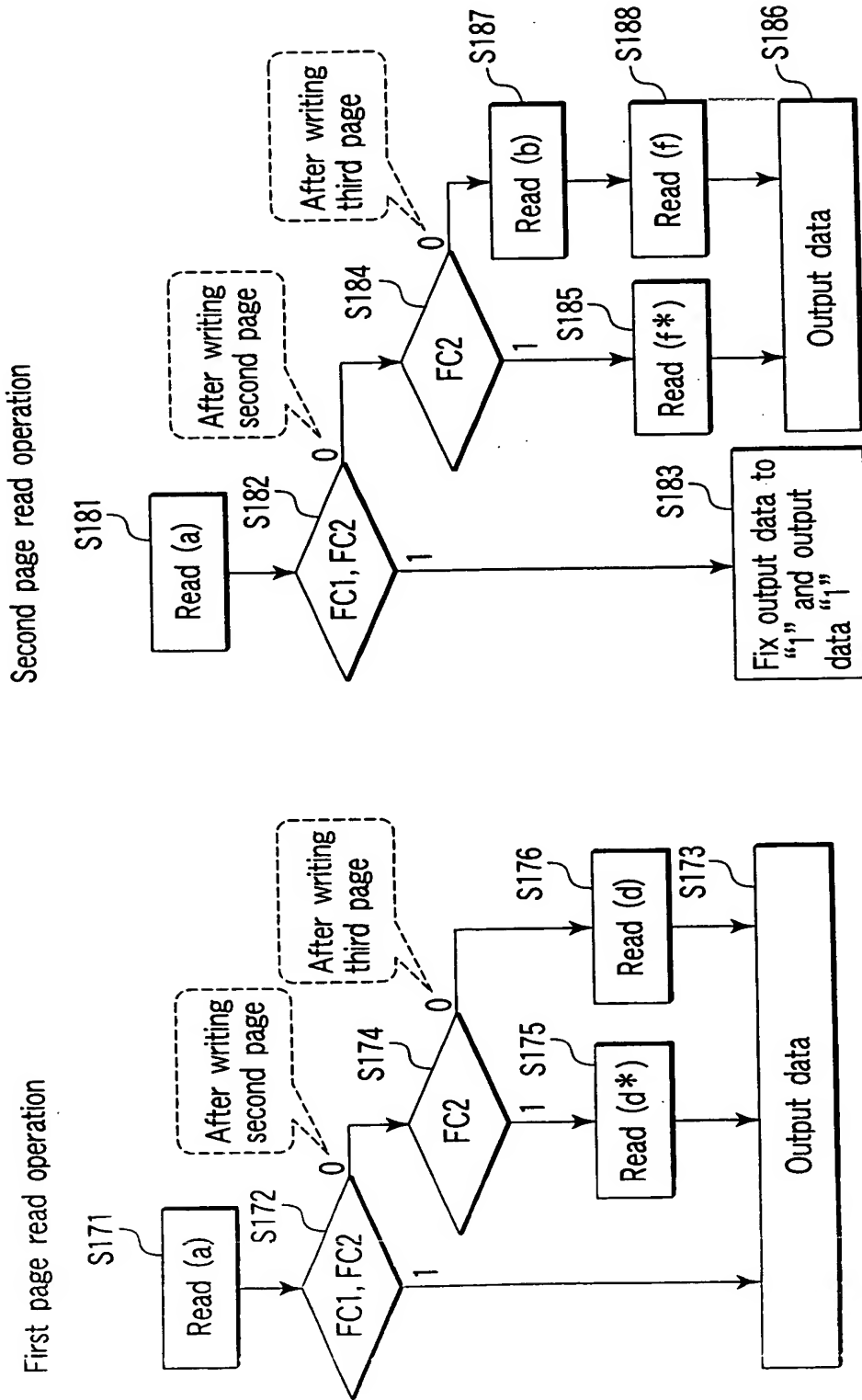
Alter third page data cache setting 2								
	Data in memory cell after writing							
	0	1	2	3	4	5	6	7
SDC	1	1	0	0	0	0	0	0
DDC	0	1	1	0	0	1	1	0
PDC	1	0	1	1	1	1	1	1
1 : Write unselected 0 : Write								

FIG. 40A

After third page data cache setting 3

After third page data cache setting 3								
	Data in memory cell after writing							
	0	1	2	3	4	5	6	7
SDC	1	1	0	0	0	0	0	0
Used for charging in verifying memory cell data 1								
DDC	0	1	1	0	0	1	1	0
Used for charging in verifying memory cell data 2								
PDC	1	0	0	0	1	1	1	1
1 : Write unselected 0 : Write								

FIG. 40B



Third page read operation

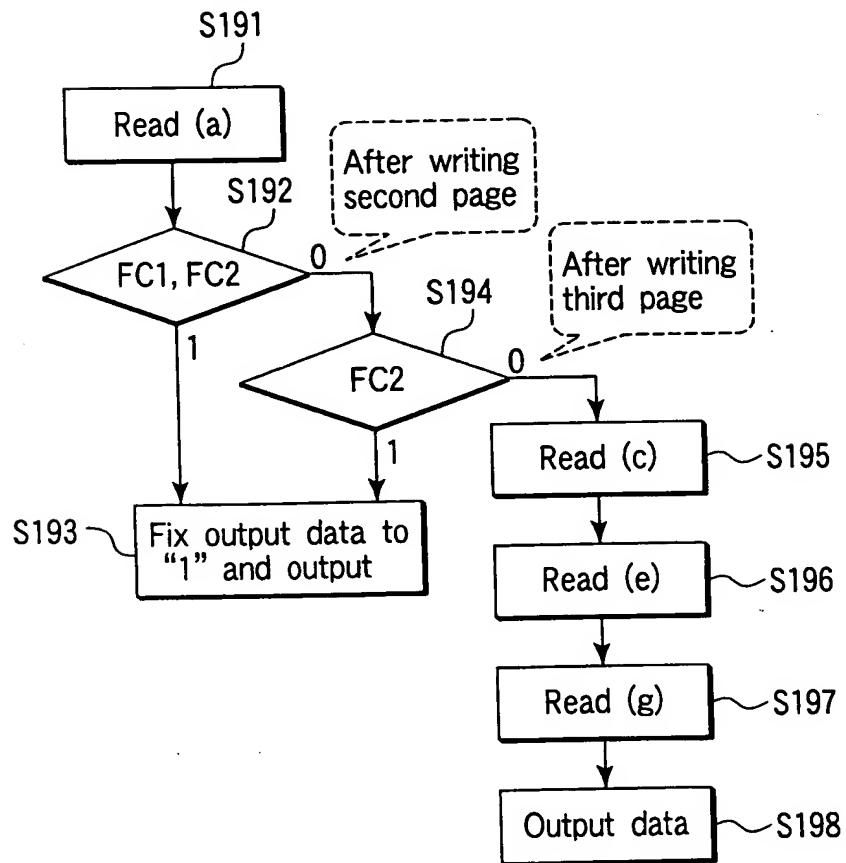


FIG. 42